INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

DEPARTMENT OF PHYSICS

(ANALOG ELECTRONICS LAB)

LAB MANUAL

CHARACTERISTICS OF FET

FET CHARACTERISTICS

AIM: a) To Draw the drain and transfer characteristics of a given FET.

b) To find the drain resistance (r_d) amplification factor (μ) and Tran conductance (g_m) of the given FET.

APPARATUS:

FET (BFW-10), Regulated power supply, Voltmeter (0-20V), Ammeter (0-100mA), Bread Board, Connecting Wires.

THEORY:

The Field Effect Transistor or Simply FET uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage, the Gates to source junction of the FET is always reversed biased. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the Field Effect Transistor a "VOLTAGE" operated device.

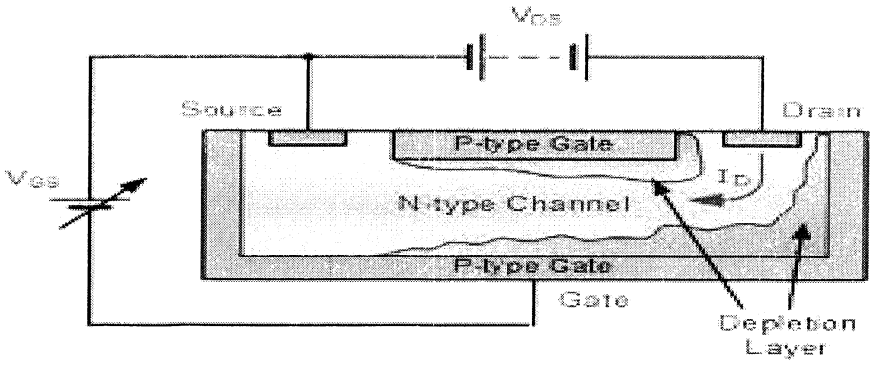
The Field Effect Transistor is a three terminal unipolar semiconductor device that has very similar characteristics to those of their *Bipolar Transistor* counterpart's i.e., high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT).

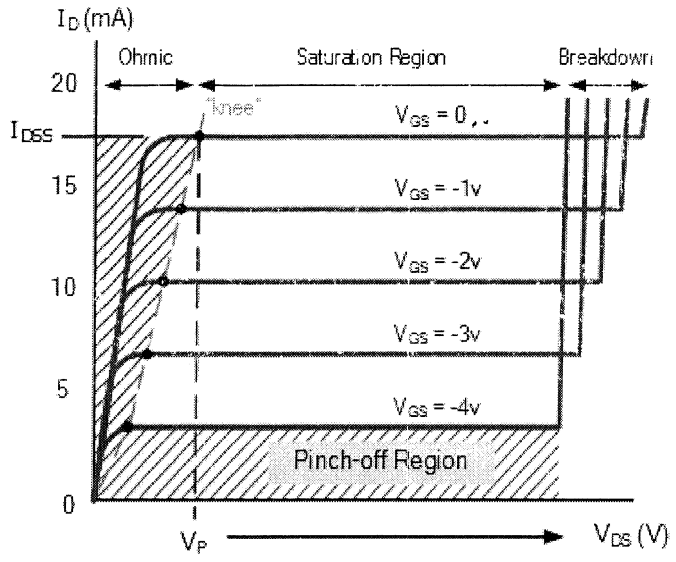
The Field Effect Transistor has one major advantage over its standard bipolar transistor, in that input impedance, (Rin) is very high, (thousands of Ohms). This very high input impedance makes them very sensitive to input voltage signals.

There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET is always reverse biased.

In amplifier application, the FET is always used in the region beyond the pinch-off.

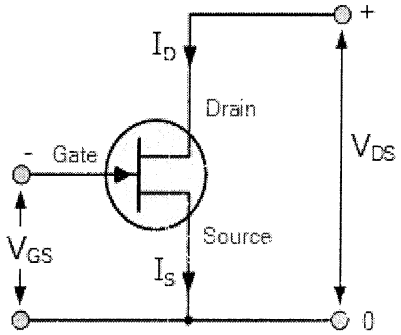




The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

• Ohmic Region-When V_{GS} =0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.

• Cut-off region- This is also known as the pinch-off region were the Gate Voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.



• Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.

• Breakdown Region-The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

In response to small applied voltage from drain to source, then n-type bar acts as simple resistor, and the drain current increases linearly with V_{DS}. With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called "pinch of voltage" (see figure).

If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage is decreased.

TRANSFER OR TRANSCONDUCTANCE CHARACTERISTICS:

Transfer characteristics are useful in evaluating the operating conditions of an FET.

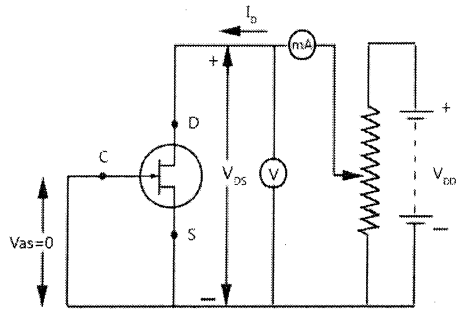
Drain current in the active region.

$$I_D = I_{DSS}^{\ 2}$$

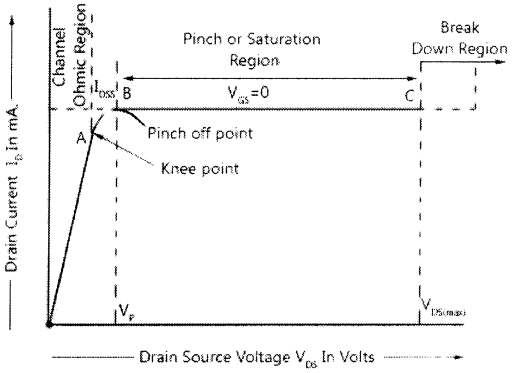
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

This is Square Law.

CIRCUIT DIAGRAM



Circuit Diagram for Determining Drain Characteristic with Shorted Gate for An N-Channel JFET



jFET Drain Characteristic With Shorted Gate

Drain Characteristics of JFET

PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. To plot the drain characteristics, keep V_{GS} constant at -1V.
3. Vary $V_{DD\ in}$ the steps of 0.2V, once current gets constant then vary V_{DD} in the steps of 1V up to 15V and observe the values of V_{DS} and I_D.
4. Repeat the above steps 2, 3 for different values of V_{GS} at -2V and -3V.
5. All the readings are tabulated.
6. To plot the transfer characteristics, keep V_{DS} constant at 1V.
7. Vary V_{GG} in the steps of 0.2V and observe the values of V_{GS} and I_D.
8. Repeat steps 6 and 7 for different values of V_{DS} at 1.5V and 2V.
9. The readings are tabulated.
10. From drain characteristics, calculate the values of dynamic resistance (r_d) by using the formula

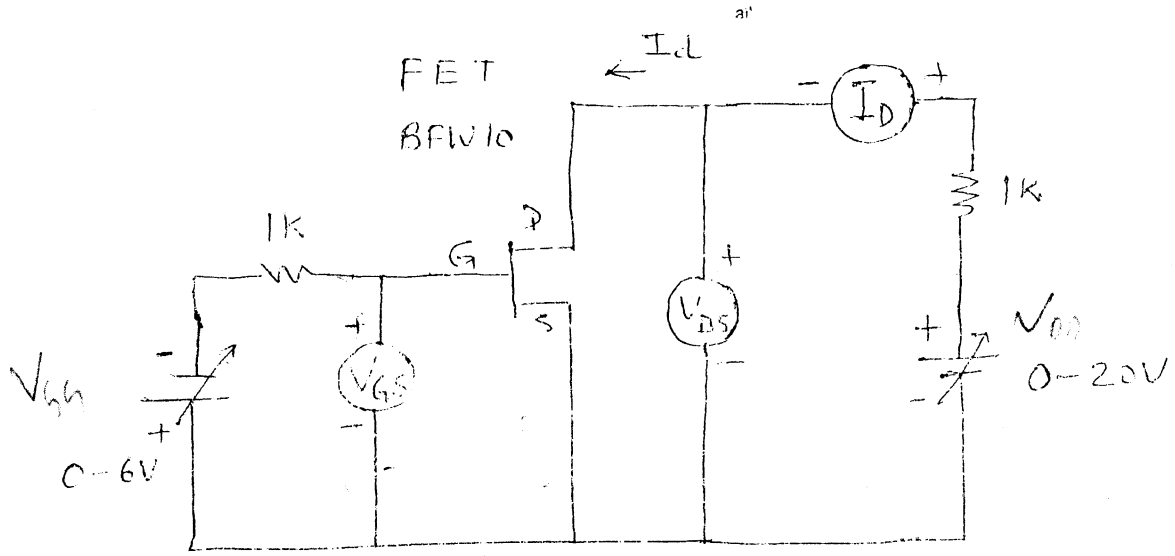
    $r_d = \Delta V_{DS} / \Delta I_D$

11. From transfer characteristics, calculate the value of trans conductance (g_m) By using the formula

    $g_m = \Delta I_D / \Delta V_{GS}$

12. Amplification factor (μ)= dynamic resistance *Tran conductance

    $\mu = \Delta V_{DS} / \Delta V_{GS}$


FET
BFW10
Id
ID
1K
1K
G
D
S
VGS
VDS
VGG
0-6V
VDD
0-20V

OBSERVATIONS:

DRAIN CHARACTERISTICS

V_{GS}= -1V		V_{GS}= -2V		V_{GS}= -3V	
V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

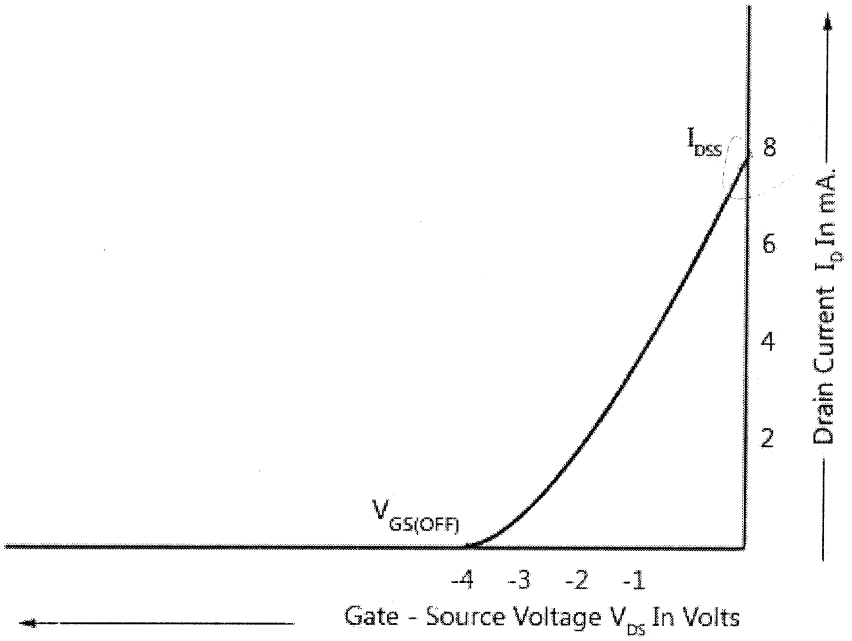
TRANSFER CHARACTERISTICS

V_{DS}=1V		V_{DS}=1.5V		V_{DS}=2V	
V_{GS} (V)	I_D(mA)	V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)

P

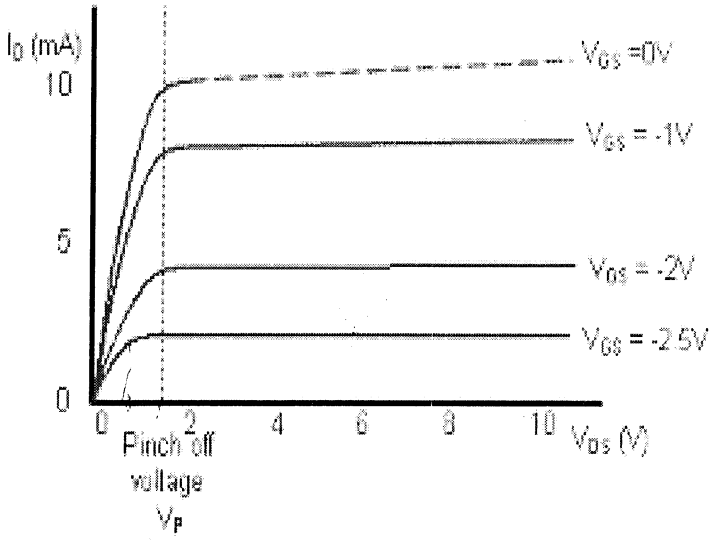
MODEL GRAPH:

TRANSFER CHARACTERISTICS



Transfer Characteristics of JFET

DRAIN CHARACTERISTICS



PRECAUTIONS:

1. The three terminals of the FET must be fully identified.
2. Practically FET contains four terminals, which are called source, drain, Gate, substrate.
3. Source and case should be short circuited.
4. Voltage exceeding the ratings of the FET should not be applied.

RESULT:

1. The drain and transfer characteristics of a given FET are drawn.
2. The dynamic resistance (r_d), amplification factor (μ) and Tran conductance (g_m) of the given FET are calculated.