INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

DEPARTMENT OF PHYSICS

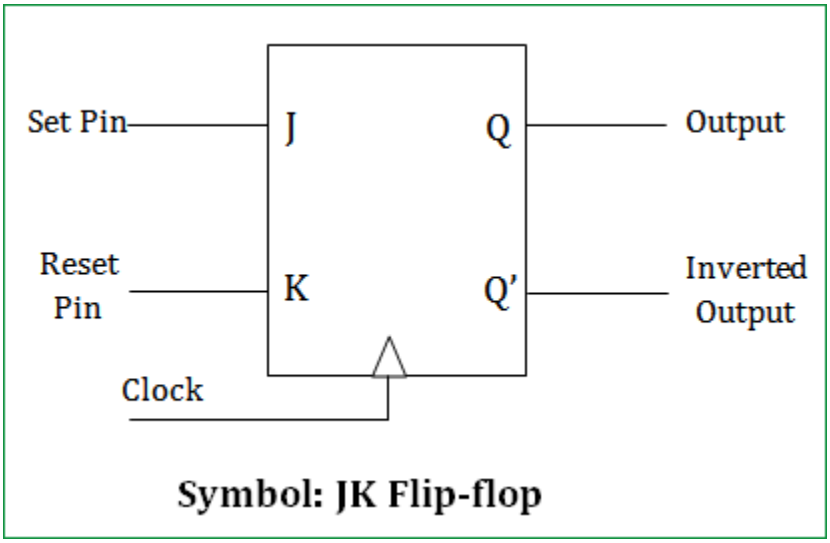
LAB MANUAL

DESIGN AND IMPLEMENTATION OF J-K FLIP FLOP

JK Flip-flop:

The name JK flip-flop is termed from the inventor Jack Kilby from texas instruments. Due to its versatility they are available as IC packages. The major applications of JK flip-flop are Shift registers, storage registers, counters and control circuits. Inspite of the simple wiring of D type flip-flop, JK flip-flop has a toggling nature. This has been an added advantage. Hence they are mostly used in counters and PWM generation, etc. Here we are using **NAND gates** for demonstrating the JK flip flop

Whenever the clock signal is LOW, the input is never going to affect the output state. The clock has to be high for the inputs to get active. Thus, **JK flip-flop is a controlled Bi-stable latch** where the clock signal is the control signal. Thus, the output has two stable states based on the inputs which have been discussed below.

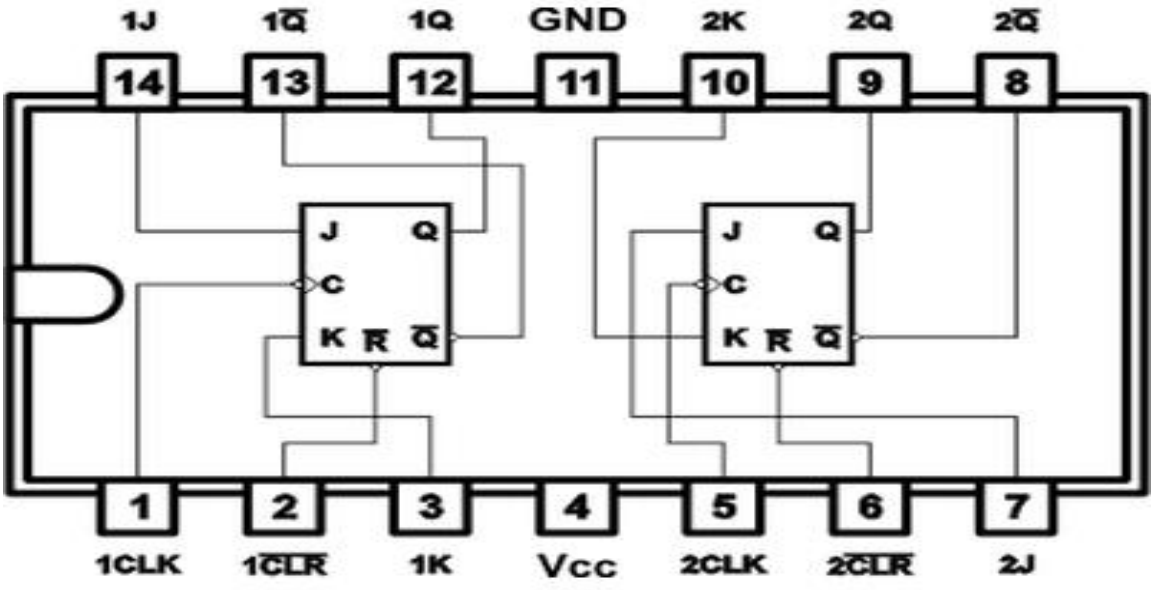


Symbol: JK Flip-flop

7473 is a commonly used Master-Slave J-K Flip-Flop IC. These ICs have two independant Master-slave Flip-Flops with two complementary outputs.

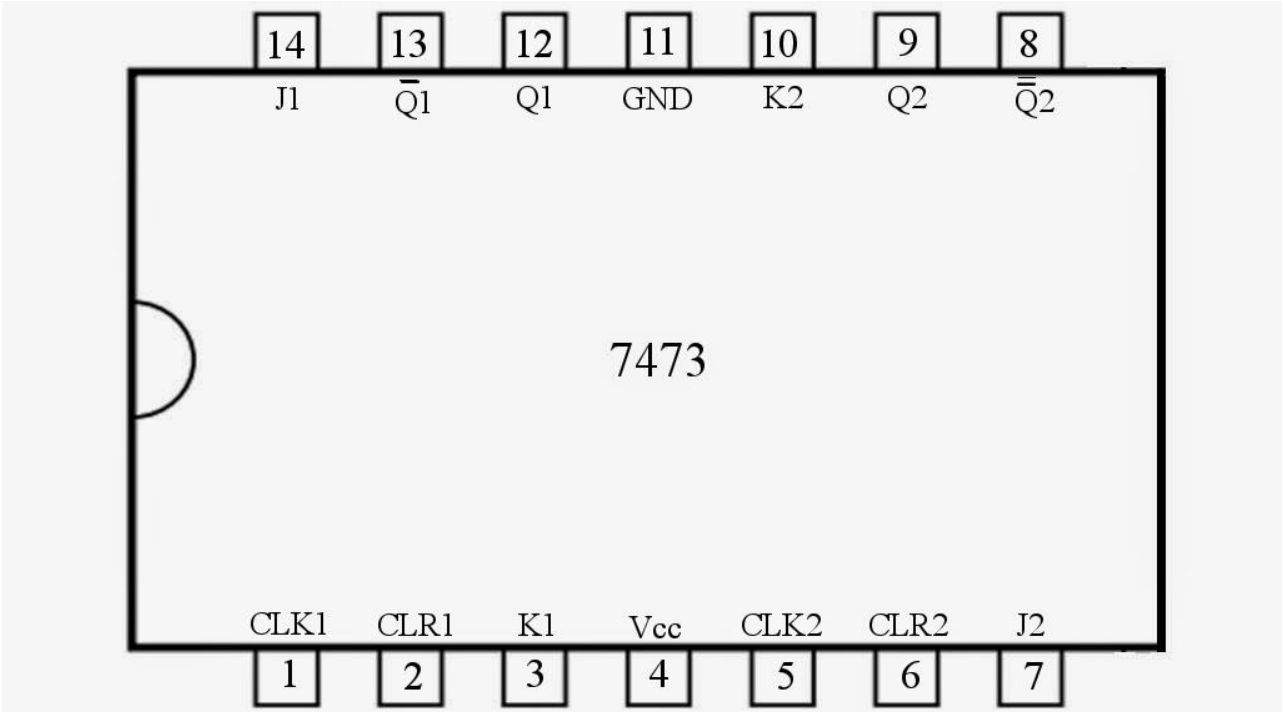
During the positive transistion of clock, data from J and K input is transferred to master and during the negative transistion of clock, data from master get transferred to the slave. If the clock is HIGH, no change will happen to the output (Q and Qbar), even if the value of J and K change. Output will change only during the negative transitions of clock. A logical LOW at CLR button will reset the outputs (Q and Qbar) and the outputs (Q and Qbar) will not change even if the J, K or CLK is changed. CLR should be set to HIGH after clearing the outputs.

Circuit diagram to put one master-slave flip-flop in circuit is given below. Input pins (J, K, CLK and CLR) of the flip-flop is connected to 5V through pull up resistors. Push button switches are connected in between the inputs (J, K, CLK and CLR) and ground. These switches helps to shift the inputs between HIGH and LOW voltages. When the switch is OFF, corresponding input will be HIGH. Similarly, if the switch is ON, corresponding input will be LOW. 5V is given from a 5V Voltage regulator. Output is connected to LEDs through current limiting resistors.



Pinout diagram of 7473

Pinout diagram of 7473 is given below. Each 7473 has two master-slave J K flip-flips. Half portion of IC, above VCC and ground constitutes the first flip-flop and the half portion below VCC and Ground constitutes the second master-slave flip-flop.



Truth Table of 7473

From the truth table, we can conclude that:

1. When CLR is LOW, Q will be LOW and Qbar will be HIGH. These outputs will not change, even if the other inputs (J, K and CLK) change, until CLR is set to HIGH.
2. When CLR becomes HIGH, if J is LOW and K is HIGH, Q becomes LOW and Qbar becomes HIGH during the next negative transition.
3. When CLR becomes HIGH, if J is HIGH and K is LOW, Q becomes HIGH and Qbar becomes LOW during the next negative transition.
4. When CLR becomes HIGH, if J and K are HIGH, Q and Qbar will toggle in each

negative transitions.
5. When CLR becomes HIGH, if J and K are LOW, Q and Qbar will remain in the previous state and is independant of the state of CLK input.

CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	L	L	Retains previous state	
H	↓	H	H	Toggle	