INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

DEPARTMENT OF PHYSICS

LAB MANUAL

# DESIGN AND IMPLEMENTATION OF T AND D FLIP FLOP.

T Flip-flop:

The name T flip-flop is termed from the nature of toggling operation. The major applications of T flip-

flop are counters and control circuits. **T flip flop is modified form of [JK flip-flop](#)** making it to operate in toggling region.

Whenever the **clock signal is LOW, the input is never going to affect the output state**. The clock has to be high for the inputs to get active. Thus, T flip-flop is a controlled Bi-stable latch where the clock signal is the control signal. Thus, the output has two stable states based on the inputs which have been discussed below.

Symbol: T Flip-flop
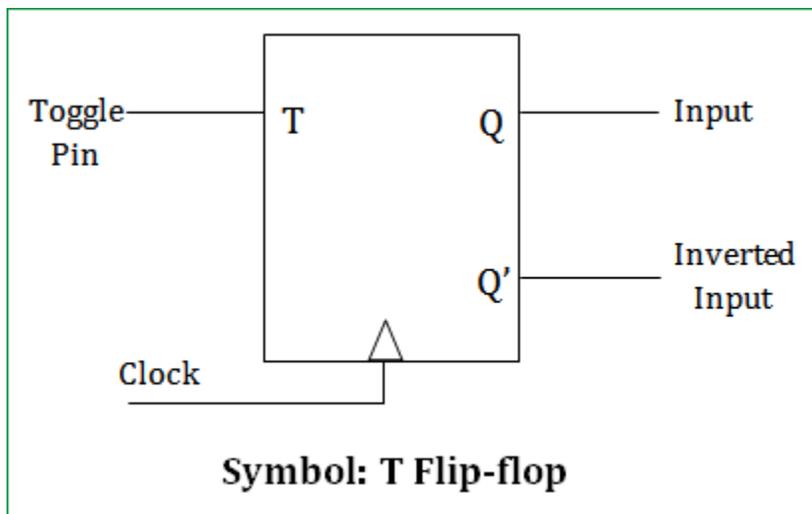
Truth Table of T Flip Flop:

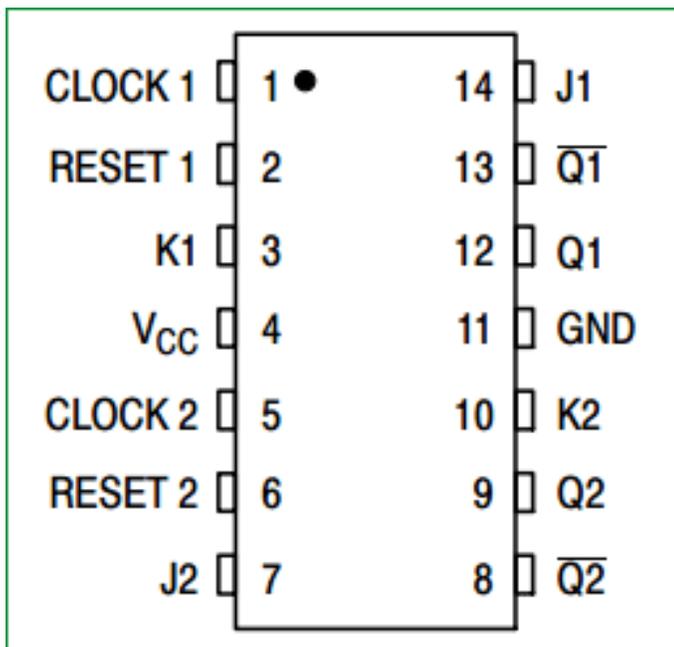| Clock	INPUT		OUTPUT	
	RESET	T	Q	Q'
X	LOW	X	0	1
HIGH	HIGH	0	No Change	

HIGH	HIGH	1	Toggle
LOW	HIGH	X	No Change

The T flip flop is the modified form of JK flip flop. The Q and Q' represents the output states of the flip-flop. According to the table, based on the input the output changes its state. But, the important thing to consider is all these can occur only in the presence of the clock signal. This, works unlike SR flip Flop & JK flip-flop for the complimentary inputs. This only has the toggling function.

RESET:

The RESET pin has to be active HIGH. All the pins will become inactive upon LOW at RESET pin. Hence, this pin always pulled up and can be pulled down only when needed.

IC Package:;

CLOCK 1 — 1 ● | 14 — J1
RESET 1 — 2 | 13 — $\overline{Q1}$
K1 — 3 | 12 — Q1
V_{CC} — 4 | 11 — GND
CLOCK 2 — 5 | 10 — K2
RESET 2 — 6 | 9 — Q2
J2 — 7 | 8 — $\overline{Q2}$

Q	True Output
Q'	Compliment Output
CLOCK	Clock Input
J	Data input 1
K	Data input 2
RESET	Direct RESET (Low activated)
GND	Ground
V_{cc}	Supply voltage

The IC used is **MC74HC73A (Dual JK-type flip-flop with RESET).** It is a 14 pin package which contains 2 individual JK flip-flop inside. Above are the pin diagram and the corresponding description of the pins. The J and K inputs will be shorted and used as **T input**.

Components Required:

1. MC74HC73A (Dual JK flip-flop) – 1No.
2. Breadboard
3. Connecting wires

D Flip Flop

In **SR NAND Gate Bistable** circuit, the undefined input condition of SET = "0" and RESET = "0" is forbidden. It is the drawback of the SR flip flop. This state:

1. Override the feedback latching action.
2. Force both outputs to be 1.
3. Lose the control by the input, which first goes to 1, and the other input remains "0" by which the resulting state of the latch is controlled.

We need an **inverter** to prevent this from happening. We connect the inverter between the Set and Reset inputs for producing another type of flip flop circuit called **D flip flop**

, Delay flip flop, D-type Bistable, D-type flip flop.

The D flip flop is the most important flip flop from other clocked types. It ensures that at the same time, both the inputs, i.e., S and R, are never equal to 1. The Delay flip-flop is designed using a gated SR flip-flop

with an inverter connected between the inputs allowing for a single input D(Data).

This single data input, which is labeled as "D" used in place of the "Set" input and for the complementary "Reset" input, the inverter is used. Thus, the level-sensitive D-type or D flip flop is constructed from a level-sensitive SR flip flop.

So, here S=D and R= ~D(complement of D)

Block Diagram
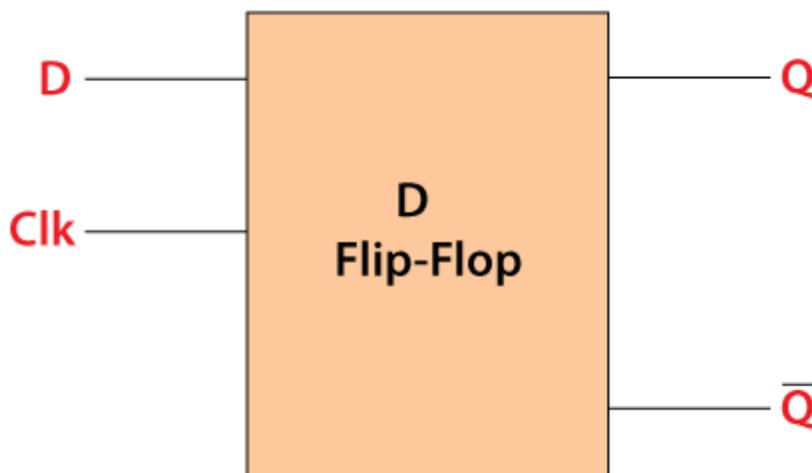
Circuit Diagram
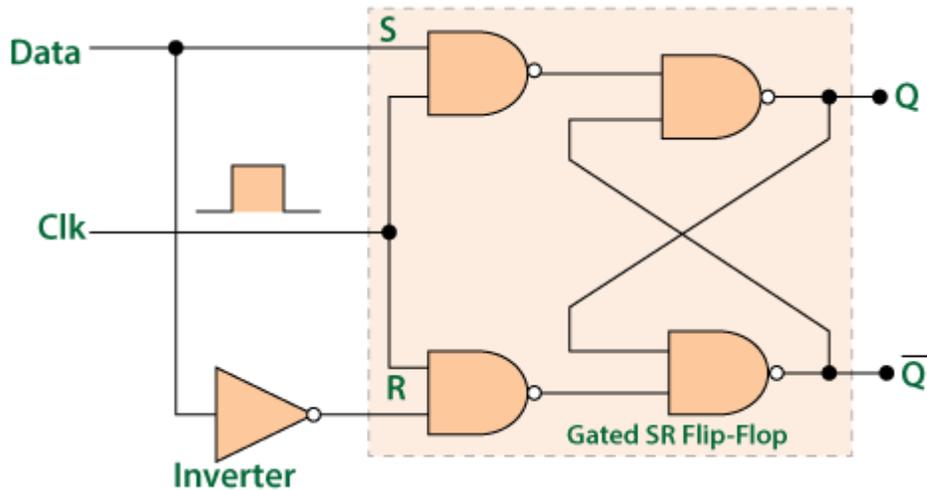
We know that the SR flip-flop requires two inputs, i.e., one to "SET" the output and another to "RESET" the output. By using an inverter, we can set and reset the outputs with only one input as now the two input signals complement each other. In SR flip flop, when both the inputs are 0, that state is no longer possible. It is an ambiguity that is removed by the complement in D-flip flop.

In D flip flop, the single input "D" is referred to as the "Data" input. When the data input is set to 1, the flip flop would be set, and when it is set to 0, the flip flop would change and become reset. However, this would be pointless since the output of the flip flop would always change on every pulse applied to this data input.

The "CLOCK" or "ENABLE" input is used to avoid this for isolating the data input from the flip flop's latching circuitry. When the clock input is set to true, the D input condition is only copied to the output Q. This forms the basis of another sequential device referred to as **D Flip Flop**.

When the clock input is set to 1, the "set" and "reset" inputs of the flip-flop are both set to 1. So it will not change the state and store the data present on its output before the clock transition occurred. In simple words, the output is "latched" at either 0 or 1.

Truth Table for the D-type Flip Flop

Clock	D	Q	Q'	Description
↓ » 0	X	Q	Q'	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

Symbols ↓ and ↑ indicates the direction of the clock pulse. D-type flip flop assumed these symbols as edge-triggers.